CLAIMS

1. An apparatus comprising:
   a switching circuit;
   a control circuit coupled to the switching circuit; and
   a biasing snubber circuit coupled to the switching circuit and the control circuit to capture energy from a circuit switched by the switching circuit and to provide at least a portion of the captured energy to bias the control circuit.

2. The apparatus of claim 1 wherein the switching circuit comprises a DC switching circuit.

3. The apparatus of claim 2 wherein the DC switching circuit comprises a buck converter circuit.

4. The apparatus of claim 2 wherein the DC switching circuit comprises a boost converter circuit.

5. The apparatus of claim 2 wherein the DC switching circuit comprises a flyback converter circuit.

6. The apparatus of claim 1 wherein the switching circuit comprises an AC switching circuit.

7. The apparatus of claim 6 wherein the biasing snubber circuit comprises first electrical circuitry to provide charge for storage on a charge storage device during a first phase of an AC flow and second electrical circuitry to provide charge for storage on the charge storage device during a second phase of the AC flow.

8. The apparatus of claim 6 wherein the AC switching circuit comprises:

a first Field Effect Transistor (FET) having a first source, a first gate and a first drain;

a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate;

a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and

a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain.

9. The apparatus of claim 6 wherein the AC switching circuit comprises:

a first Field Effect Transistor (FET) having a first source, a first gate and a first drain;

a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate;

a first diode having a first cathode coupled to the first source and a first anode coupled to the first drain; and

a second diode having a second cathode coupled to the second source and a second anode coupled to the second drain.

10. The apparatus of claim 6 wherein the biasing snubber circuit comprises:

a first and second series resistor/capacitor pair correspondingly coupled to a first and a second drain of a first and a second Field Effect Transistor (FET) of the AC switching circuit;

a first diode coupled between a first source of the first FET and the first series resistor/capacitor pair, an anode of the first diode coupled to the first source and a cathode of the first diode coupled to the first series resistor/capacitor pair;

a second diode coupled between a second source of the second FET and the second resistor/capacitor pair, an anode of the second diode coupled to the second source and a cathode of the second diode coupled to the second series resistor/capacitor pair;

a third diode, an anode of the third diode coupled to the cathode of the first diode;

a fourth diode, an anode of the fourth diode coupled to the cathode of the second diode and a cathode of the fourth diode coupled to a cathode of the third diode; and

a capacitor coupled between coupled cathodes of the third and fourth diodes and the first and second sources, the first and second sources coupled together.

11. The apparatus of claim 6 wherein the biasing snubber circuit comprises:

a first terminal of a first capacitor and a first terminal of a second capacitor correspondingly coupled to a first and a second drain of a first and a second Field Effect Transistor (FET) of the AC switching circuit;

a first series linear-device/diode pair coupled between a second terminal of the first capacitor and a first source of the first FET;

a second series linear-element/diode pair coupled between a second terminal of the second capacitor and a second source of the second FET;

a first diode, wherein an anode of the first diode is coupled to the second terminal of the first capacitor;

a second diode, wherein an anode of the second diode is coupled to the second terminal of the second capacitor and a cathode of the second diode is coupled to a cathode of the first diode; and

a bias capacitor coupled between coupled cathodes of the first and second diodes and the first and second sources, the first and second sources coupled together.

12. The apparatus of claim 11 wherein the first series linear-device/diode pair comprises a first resistor and a third diode and the second series linear-device/diode pair comprises a second resistor and a fourth diode.

13. The apparatus of claim 11 wherein the first series linear-device/diode pair comprises a first inductor and a third diode and the second series linear-device/diode pair comprises a second inductor and a fourth diode.

14. The apparatus of claim 13 wherein anodes of third and fourth diodes are coupled to the coupled sources and cathodes of the third and fourth diodes are correspondingly coupled to the first and the second inductors.

15. The apparatus of claim 11 wherein the biasing snubber circuit further comprises:

a first terminal of a first resistor and a first terminal of a second resistor correspondingly coupled to the anode of the first diode and the anode of the second diode;

a full wave diode bridge rectifier having four bridge diodes, wherein a first terminal of the full wave bridge rectifier coupled to the bias capacitor, a second terminal of the full wave bridge rectifier coupled to a second terminal of the first resistor, a third terminal of the full wave bridge rectifier coupled to a second terminal of the second resistor and a fourth terminal of the full wave bridge rectifier coupled to a ground node, the ground node comprising the coupled first and second sources.

16. The apparatus of claim 11 wherein the biasing snubber circuit further comprises:

a first resistor wherein a first terminal of the first resistor is coupled to the first terminal of the first capacitor and a second terminal of the first resistor is coupled to the second terminal of the first capacitor; and

a second resistor wherein a first terminal of the second resistor is coupled to the first terminal of the second capacitor and a second terminal of the second resistor is coupled to the second terminal of the second capacitor.

17. The apparatus of claim 6 further comprising a load coupled to the AC switching circuit.

18. The apparatus of claim 17 wherein the load comprises an inductive heating device.

19. The apparatus of claim 17 wherein the load comprises a single phase induction motor.

20. The apparatus of claim 17 wherein the load comprises a fuser.

21. An imaging system comprising:
a processor;
a networking interface; and
an imaging subsystem coupled to the processor, the imaging subsystem including:
a switching circuit;
a control circuit coupled to the switching circuit; and
a biasing snubber circuit coupled to the switching circuit and the control circuit, wherein the biasing snubber circuit captures energy from a circuit switched by the switching circuit and wherein biasing snubber circuit provides at least a portion of the captured energy to bias the control circuit.

22. The imaging system of claim 21 wherein the switching system comprises an AC switching system.

23. The imaging system of claim 22 wherein the AC switching circuit comprises:

a first Field Effect Transistor (FET) having a first source, a first gate and a first drain;

a second FET having a second drain, a second source coupled to the first source and a second gate coupled to the first gate;

a first diode having a first anode coupled to the first source and a first cathode coupled to the first drain; and

a second diode having a second anode coupled to the second source and a second cathode coupled to the second drain.

24. The imaging system of claim 22 wherein the biasing snubber circuit comprises first electrical circuitry to provide charge for storage on a charge storage device during a first phase of an AC flow and second electrical circuitry to provide charge for storage on the charge storage device during a second phase of the AC flow.

25. The imaging system of claim 22 wherein the biasing snubber circuit comprises:

a first terminal of a first capacitor and a first terminal of a second capacitor correspondingly coupled to a first and a second drain of a first and a second Field Effect Transistor (FET) of the AC switching circuit;

a first series linear-device/diode pair coupled between a second terminal of the first capacitor and a first source of the first FET;

a second series linear-device/diode pair coupled between a second terminal of the second capacitor and a second source of the second FET;

a first diode, wherein an anode of the first diode is coupled to the second terminal of the first capacitor;

a second diode, wherein an anode of the second diode is coupled to the second terminal of the second capacitor and a cathode of the second diode is coupled to a cathode of the first diode; and

a bias capacitor coupled between coupled cathodes of the first and second diodes and the first and second sources, the first and second sources coupled together.

26. The imaging system of claim 25 wherein the first series linear-device/diode pair comprises a first inductor and a third diode and the second series linear-device/diode pair comprises a second inductor and a fourth diode.

27. The imaging system of claim 22 further comprising a load coupled to the AC switching circuit.

28. The imaging system of claim 27 wherein the load comprises an inductive heating device.

29. The imaging system of claim 27 wherein the load comprises a single phase induction motor.

30. The imaging system of claim 27 wherein the load comprises a fuser.

31. A snubber circuit comprising:

a first energy storage device;

circuitry coupled to the first energy storage device to facilitate capturing, by the first energy storage device, energy of a switching circuit and to facilitate resetting of the first energy storage device; and

a second energy storage device coupled to the first energy storage device to store the captured energy.

32. The snubber circuit of claim 31 wherein the switching circuit is a DC switching circuit.

33. The snubber circuit of claim 31 wherein the switching circuit is an AC switching circuit.

34. The snubber circuit of claim 31 wherein the circuitry comprises a plurality of diodes.

35. The snubber circuit of claim 31 wherein the second energy storage device provides a bias source for a control circuit of the switching circuit..

36. The snubber circuit of claim 31 wherein the second energy storage device provides a bias source for a fan.

37. The snubber circuit of claim 31 wherein at least one of the first and second energy storage devices comprises a capacitor.

38. The snubber circuit of claim 31 wherein at least one of the first and second energy storage devices comprises an inductor.

39. A method of supplying power to a first circuit comprising:

capturing energy of a switching circuit in a first energy storage device;

providing at least a portion of the captured energy in the first energy storage device to a second energy storage device; and

providing at least a portion of energy stored on the second energy storage device to power the first circuit.

40. The method of claim 39 wherein the first circuit comprises a control circuit for the switching circuit.

41. The method of claim 39 wherein the switching circuit comprises an AC switching circuit.

42. The method of claim 39 wherein the switching circuit comprises a DC switching circuit.

43. A snubber circuit to power a first circuit comprising:

means for capturing energy of a switching circuit in a first energy storage device;

means for providing at least a portion of the captured energy in the first energy storage device to a second energy storage device; and

means for providing at least a portion of energy stored on the second energy storage device to power the first circuit.

44. The snubber circuit of claim 43 wherein at least one of the first energy storage device and the second energy storage device comprise capacitors.

45. The snubber circuit of claim 43 wherein the first circuit comprises a control circuit for controlling the switching circuit.